Searching PAJ 1/1 ページ

PATENT ABSTRACTS OF JAPAN

(11)Publication number: 2000-151640(43)Date of publication of application: 30.05.2000

(51)Int.Cl. H04L 12/28 H04L 29/14

H04Q 3/00

(21)Application number : 10-323750 (71)Applicant : OKI ELECTRIC IND CO LTD

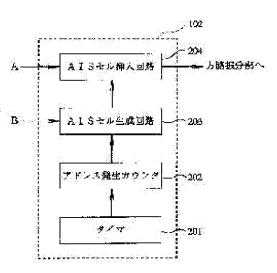
(22)Date of filing: 13.11.1998 (72)Inventor: KAWACHI HAJIME

(54) ATM SYSTEM

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the scale of hardware by eliminating the need for a connection setting table for an alarm indication signal.

SOLUTION: An address generating counter 202 conducts countup or countdown based on a period given from a timer 201 to generate sequentially virtual paths. An alarm indication signal AIS cell generating circuit 203 uses the virtual paths received from the address generating counter 202 to sequentially generate AIS cells. An AIS cell insertion circuit 204 transmits sequentially the AIS cells to a path distribution section for a user cell. An alarm generating section 102 generates alarm indication cells for all addresses and transmits them and invalid cells are discarded to a path distribution section for the user cell. Thus it is not required to provide the connection setting table to the alarm generating section 102.



LEGAL STATUS

[Date of request for examination]

15.01.2002

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3640551 [Date of registration] 28.01.2005

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]